

Aurora SwitchKit™ Product Brief

Features

- From 2 to 24 Aurora ports, any mix of lane configurations.
- Aurora Protocol Specification version 1.3 compliant.
- Optional credit based flow-control scheme for congestion handling.
- Supports 8, 10, 12, 14 or 16-bit source and destination IDs.
- Multicast port group support.
- Aggregate port group support for trunking and load balancing applications.
- Supports four or eight traffic priority levels.
- Supports optional error detection and logging.
- Optional Error Detection And Correction (EDAC) on all memory structures.

Description

The switch provides wire-speed, non-blocking connectivity between Aurora link layer ports. The Switch Management Block supports in-band accesses to internal registers, as well as generating error and status event notification messages.

The switch core interfaces to Aurora interface cores through 16, 32, or 64-bit LocalLink interfaces. The Aurora link layer interface cores are generated by the ISE 8.1i Core Generator tool, and encapsulated with a Praesum supplied wrapper.

Figure 1 illustrates the overall architecture of the switch.

Supported Standards

Lite Transport Layer Specification.
Aurora Protocol Specification.

Figure 1 Aurora Switch Block Diagram

