RapidIO® 2.x LP-Serial Physical Layer Endpoint Core - Product Brief

Features

- Implements the complete RapidIO Physical Layer LP-Serial protocol.
- Compliant with Rev. 2.2 of the specification
- Implements RapidIO Error Management Extensions
- Supports 1x, 2x, and 4x link widths.
- Hardware error recovery.
- Flexible SERDES interface supports industry standard serial transceiver blocks.
- Integrated buffer module for transmit and receive packet buffering.
- AXI4 IO Logical Layer Target and Initiator interfaces.
- Management Entity with integrated decoder for RapidIO maintenance transactions.
- Management Entity supports optional soft packet interface which enables software implementations of logical layer functions.

Description

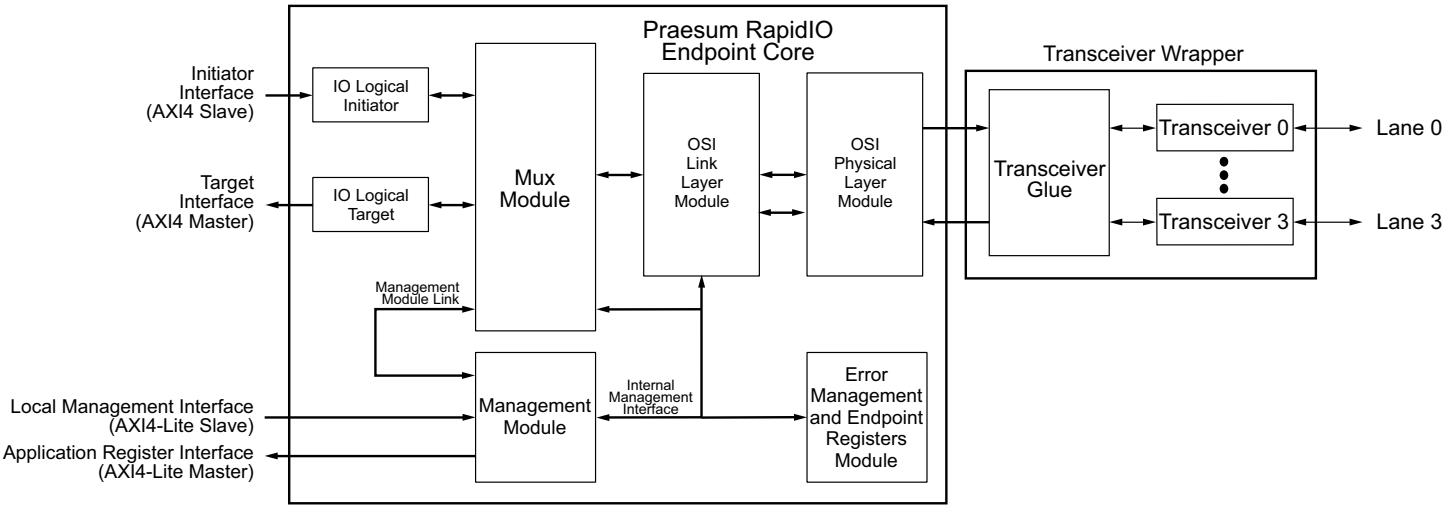
The LP-Serial Endpoint Core implements all of the functions are defined in the RapidIO Physical Layer LP-Serial Specification Rev. 2.2. Figure 1 illustrates the overall architecture of the core.

The core integrates an IO Logical Layer Initiator that maps AXI4 transactions into RapidIO IO Logical request packets. The user interface consists of a 64-bit or 128-bit AXI4 slave interface.

The core also integrates an IO Logical Layer Target that maps RapidIO IO Logical request packets into AXI4 transactions on the user interface. This user interface consists of a 64-bit or 128-bit AXI4 master interface.

In addition to the RapidIO Physical layer functions, the core also includes Management Module that supports access to Physical, Transport, and Logical Layer CSRs either through maintenance transactions, or through the AXI4-lite Local Management Interface (LMI).

Figure 1 RapidIO® 2.x LP-Serial Physical Layer Endpoint Core Block Diagram



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