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Praesum SwitchKit™

SwitchKit Overview

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- SwitchKit is an IP Tool Kit for creating application specific switches in ASICs or FPGAs.
- SwitchKit core components are generic and can be used to support any packet or cell based protocol.
- Application specific personality modules are added for specific protocols.
- Delivered as:
  - RTL Source
  - Netlists for FPGAs

Why SwitchKit?

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- Ability to quickly create a switch optimized for the target application with customized:
  - Port count
  - Port types
  - Embedded peripherals
  - End-point addressable memory
  - Management interfaces
  - Protocol bridges
  - Traffic handling for:
    - Multicast
    - Traffic patterns that are important to the application

SwitchKit Components

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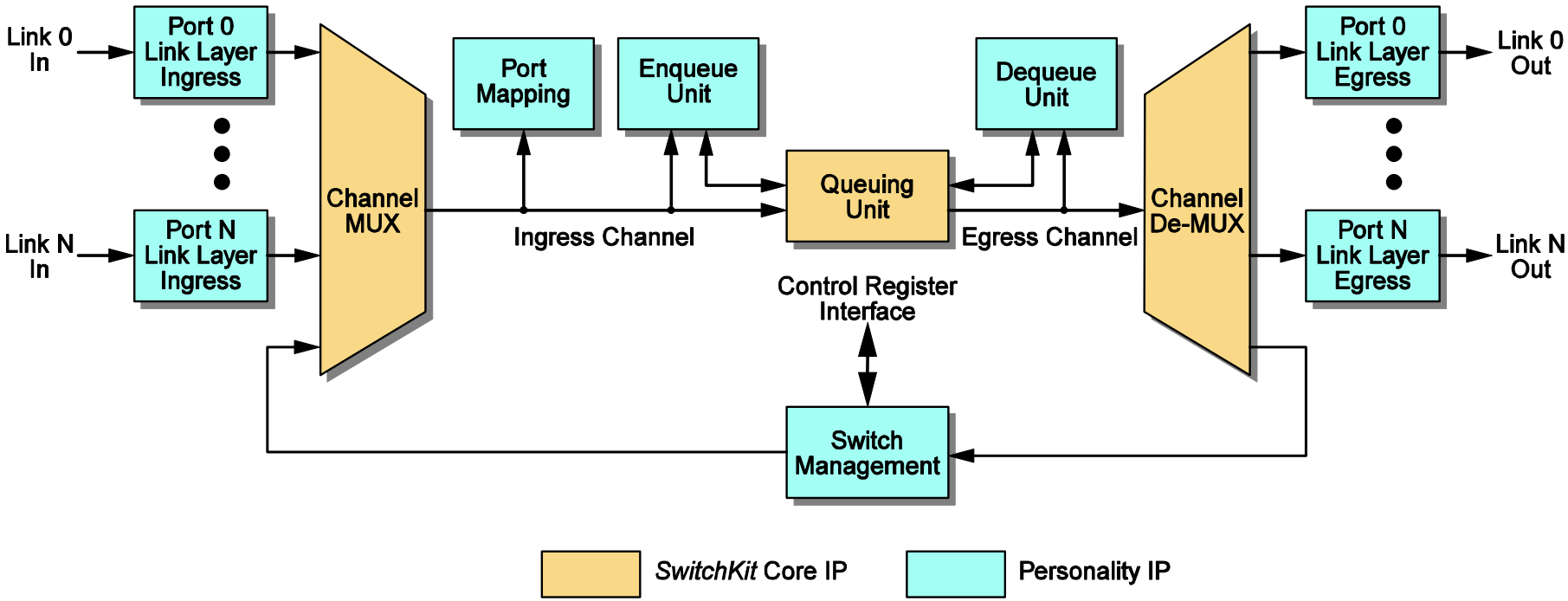
- Channel Mux & Demux
  - Aggregates traffic from ports to and from queuing unit
- Queuing Unit
  - Manages traffic flow queues under control of application specific Enqueue and Dequeue units
  - Use models
    - Storage for central memory switch
    - Ingress and egress queues for crossbar switch
- Crossbar & Arbiter (Available 2H 06)
  - Provides space switching function for larger switches

Shared Memory Switch Architecture



Application Specific Blocks

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- Protocol specific blocks
  - Port Mapping Unit - Maps incoming PDUs to traffic flows based on such factors as:
    - Destination address
    - Explicit priority indication
  - Enqueue Unit – Links packets to queues
  - Dequeue Unit – Unlinks packets, and implements forwarding policy
  - Link and Physical Layer – Ingress and egress port functions

SwitchKit Personality Rollout

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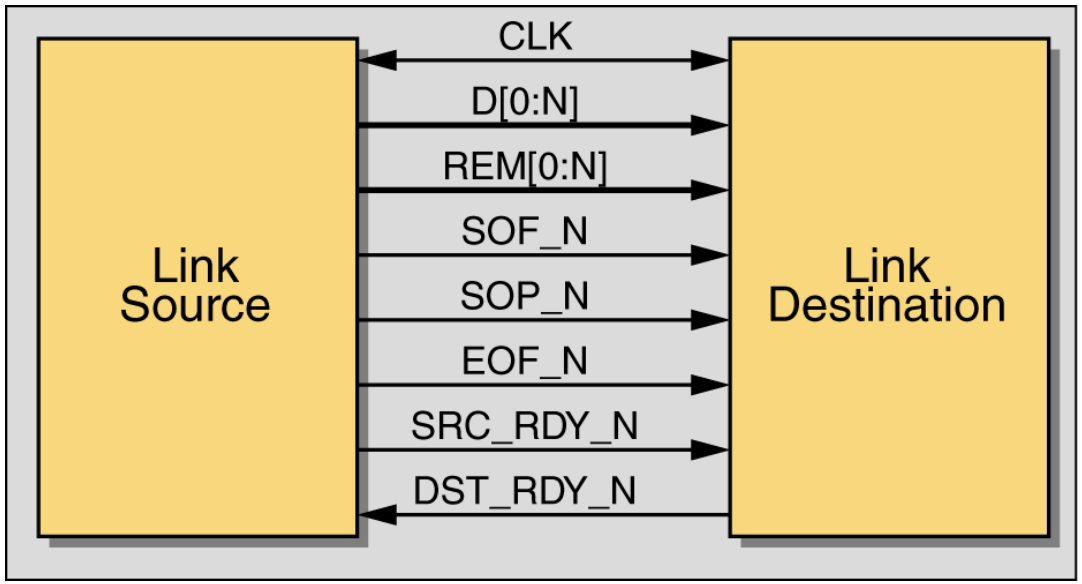
- Currently four standard personalities are planned
  - RapidIO *SwitchKit*
    - Available now
    - Being deployed by customer in ASIC
  - Aurora *SwitchKit*
    - Available now in V-4
    - Being ported to V-5
  - Ethernet *SwitchKit*
    - Q3/06
  - PCI Express *SwitchKit*
    - Q4/06
- Others will be rolled out based on customer demand

LocaLink™ Interface



- Used to transfer data between blocks
- Point to point, half duplex interface
- Interface extensions via:
  - Sideband signals
  - PDU tags

Verification & Validation

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- Three pronged approach
  - Extensive Simulation
    - Using “golden” traffic generators
    - Extensive use of randomization
    - Moving towards hardware acceleration
  - Hardware Verification in FPGAs on ATCA platform
    - Uses the same traffic generation as simulation environment
    - Accelerates verification
  - Hardware Validation with Golden Hardware
    - Freescale 8540 for Parallel RapidIO
    - Freescale 8548 for Serial RapidIO

Regression Testing

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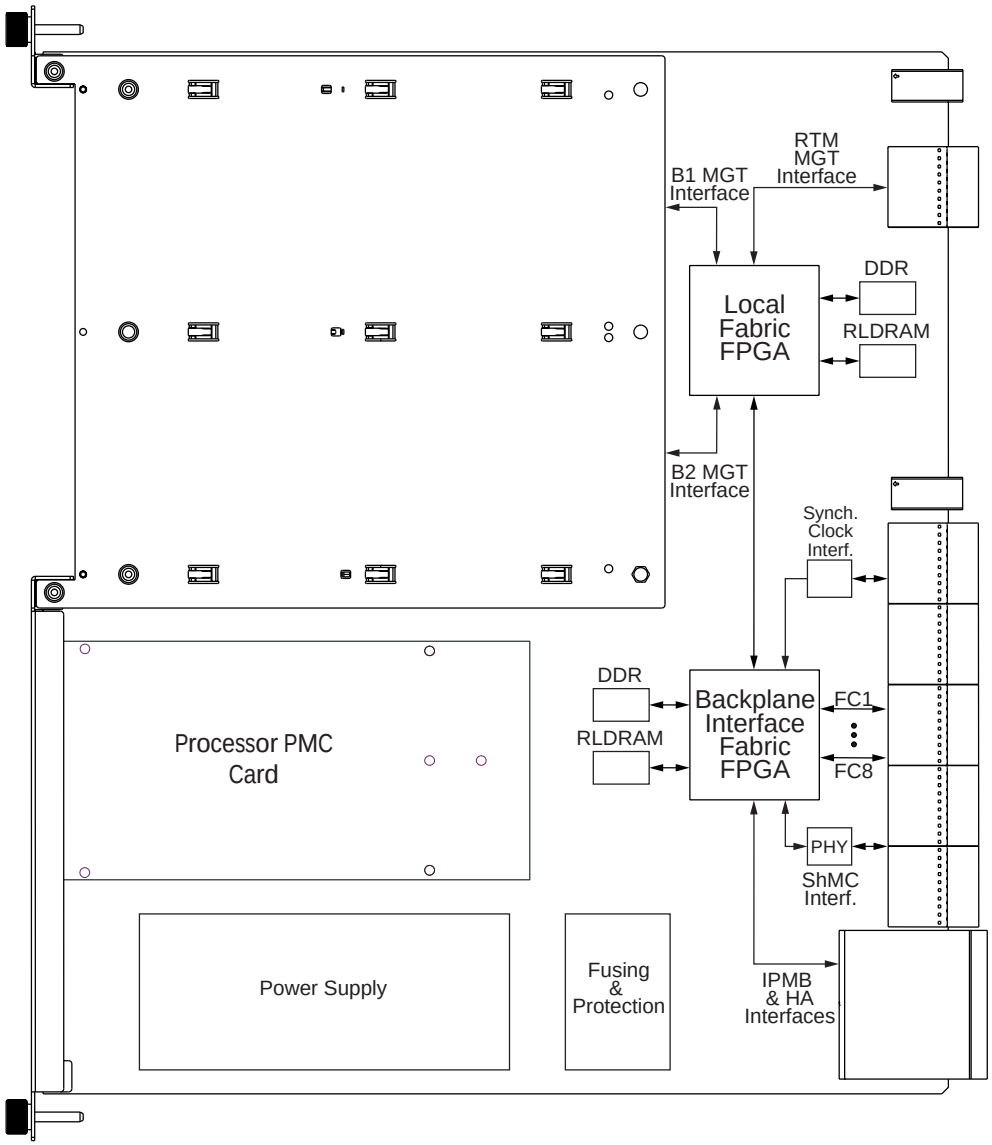
- All switches are run through a fully automated regression suite before release.
- Suit runs for approx. 3 days for Parallel RapidIO
  - Runtimes are approx. 1 week for serial protocols due to SERDES model overhead.
- Suite tests include:
  - Data plane forwarding including:
    - Transient congestion
    - Over-subscribed port congestion
  - Control plane traffic handling
  - Exhaustive testing of control registers
  - Multicast handling including multicast rate limiting
  - Error handling and reporting

ATCA Validation Platform



- Backplane Interface Fabric FPGA
  - Implements Full-Mesh backplane interface.
- Local Fabric FPGA for switching between
  - Advanced Mezzanine Card (AMC) bays
  - Rear Transition Module (RTM)
  - Backplane Interface
- Processor PMC for system management

Summary: SwitchKit Value Proposition

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- Shorter Time to Market
  - Solid base of switching IP for you build your value added IP on.
- Lower Cost.
  - Development and maintenance costs spread over entire customer base.
- A Better starting point.
  - More Flexible
  - More Mature
  - Better Debug support
  - Growth path