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Warthog Flex HPCS

Arria 10 SoC HPEC Tile

Features

- Arria 10 SoC FPGA Processing Element (PE) containing:
  - 1.5 GHz Dual Core ARM® Cortex™-A9 plus 660K FPGA Logic Elements
  - 1.5 TFLOPS of single precision floating point hardware, operating at 50 GFLOPS per watt.
  - 64 GB of DDR4 memory with ECC.
- Transceiver based computing interfaces for expansion:
  - RapidIO full-mesh cluster interface supporting 3 to 7 links.
  - Dual 10 Gbit Ethernet interfaces
  - PCIe Gen 3 x8 interface for host attachment or IO expansion.
- Linux OS support with optimized libraries including:
  - Open MPI
  - BLAS
- Fully supported by the Warthog OpenCL development environment.

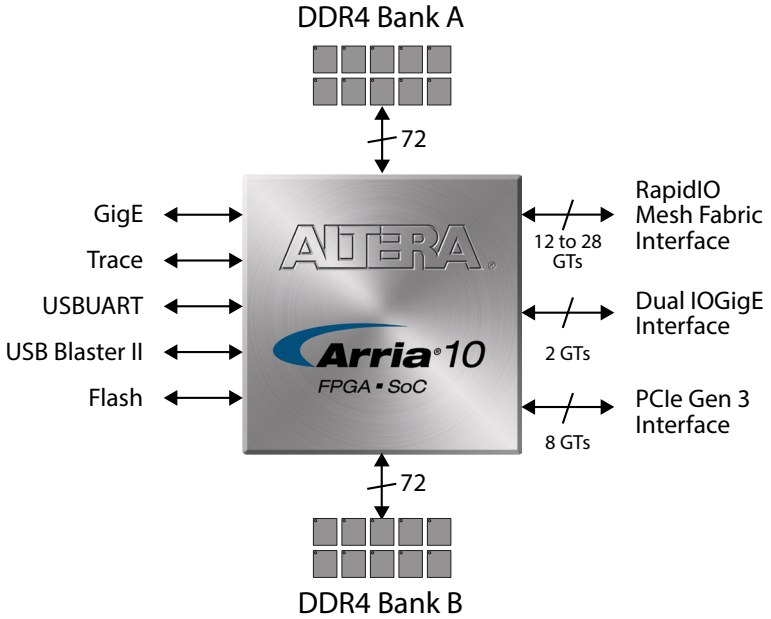
Description

The A10 SoC Tile provides high performance ARM + FPGA processing capabilities for High Performance Embedded Computing (HPEC) systems.

It provides unprecedented IO flexibility for processing both streaming data and shared memory datasets.

The tile is delivered as a complete package consisting of: an optimized layout, OpenCL and cluster computing IP for the FPGA, and Linux operating system plus optimized HPC libraries. Multiple tiles can be combined to scale computing throughput over a wide range.

Figure 1 Warthog Flex A10 SoC Tile Block Diagram



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